NAJATH AKRAM, PH.D.

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SUMMARY

Signal processing engineer, ten years in wireless, the last six on LTE and 5G NR O-RAN radio units. At Airspan, owns the bit-accurate DFE and low-PHY reference models that firmware is signed off against, and the lab team's fronthaul test tools; at Jabil, wrote the DFE architecture and 3GPP implementation specifications. Ph.D. dissertation in reduced-hardware beamforming receivers; 10+ IEEE publications.

CORE SKILLS

Wireless systems: 5G NR and LTE physical layer; O-RAN fronthaul (split 7.2x, WG4 CUS-plane, eCPRI, BFP compression); 3GPP TS 38.211, 38.104, 38.141 and 36.141; multiband TDD and FDD radio unit architecture; EVM, ACLR, OBUE and PIM analysis

DSP and modeling: DFE design (DUC and DDC, NCO, channel and pulse-shaping filters, interpolation and decimation chains); CFR and cancellation-pulse design; PRACH detection; fixed-point and bit-exact modeling against vendor IP C-models; BFP codecs

Platforms and tools: MATLAB (5G, LTE and HDL toolboxes, App Designer, Compiler); AMD/Xilinx RFSoC and DFE IP; Python; Keysight 89600 VSA

AI engineering: Anthropic Claude API and Agent SDK; multi-agent pipelines with schema-validated outputs; per-call cost ledgers and budgets; evaluation harnesses; TypeScript, Next.js, PostgreSQL

EXPERIENCE

AIRSPAN NETWORKS — Houston, Texas

Signal Processing Engineer — *January 2025 to present*

O-RAN 7.2x radio units: bit-accurate DFE and low-PHY reference modeling, FPGA IP verification, and fronthaul test tooling.

- Developed and maintain the bit-accurate DL/UL DFE + low-PHY reference models that generate the RTL golden vectors, so RTL is compared bit for bit rather than to a tolerance: NR/LTE test models through IFFT/FFT, CFR, the Xilinx channel-filter/mixer IP C-models, and O-RAN BFP at 8/9/10/12/14-bit, across 3-100 MHz including combined-band carriers (e.g. B28+B20).
- Built the bit-accurate PRACH receive-chain model (Xilinx PRACH DDC and decimation, CP removal, FFT, subcarrier extraction, BFP and U-plane packing, detection) covering every LTE format and all NR FR1 formats, L_{RA} 839 and 139, FDD and TDD.
- Built an O-RAN fronthaul power and PAPR tool: per-eAxC dBFS power, grid-domain PAR, per-tone PAR, and oversampled time-domain PAPR reported separately, auto-detecting BFP width and eAxC bit split and deriving the compressed-domain full-scale reference per O-RAN WG4 CUS 8.1.3.1. Shipped as MATLAB Compiler GUI and CLI executables plus a Python version.
- Built an uplink EVM and PRACH analyzer that demodulates PUSCH and PRACH from 7.2x U-plane captures, with views aligned to the Keysight 89600 VSA, and an RU-to-DU full-scale alignment check that emulates the DU's fixed-point ingest (shift, container width, wrap or saturate) against the per-PRB BFP exponents to separate RU misconfiguration from DU ingest error.
- Built the expected versus captured IQ comparison GUI used in bring-up: cross-correlation delay alignment, overlaid PSD and PSD difference, and dBFS power readout for hex, BFP, mat, and raw binary captures.
- Re-clocked CFR from 491.52 to 245.76 MSPS and redesigned the cancellation pulses and channel filters for 3 to 20 MHz (a 3 MHz channel filter is not realizable at 30.72 MSPS) to meet an operator's 3 MHz carrier requirement, tuning cutoff and pulse length against a per-symbol constellation EVM metric rather than the vendor's RMS figure: 2.17 to 2.23% EVM at 3, 5, and 10 MHz inside ACLR and OBUE margin.
- Built a multiband PIM planner that catalogs IM3, IM5, and IM7 products for multi-carrier downlink and flags uplink-band hits; checked by hand against a B71, B29, and B14 stack.

JABIL INC. — Warren, New Jersey and Houston, Texas

Principal Wireless Systems Design Engineer — *December 2023 to August 2024*

Lead Wireless Systems Design Engineer — *September 2021 to December 2023*

Senior FPGA Design Engineer — *December 2020 to September 2021*

- Led the software and firmware workstreams for LTE and 5G NR O-RAN radio units from single-band to tri-band through commercial release: defined NR implementation requirements, wrote the architecture and implementation documents the digital design team built to, weighed massive MIMO and O-RAN functional-split options against implementation complexity, resources, and timelines, and briefed customers on passive intermodulation.
- Primary author of the DFE System Design Documents for two radio lines, a B3 FDD radio (5 to 40 MHz) and a 100 MHz TDD radio: the interpolation chain to 983.04 MSPS, pulse-shaping filters derived from TS 38.104 guard-band rules and grouped into five classes covering thirteen bandwidths, CFR cancellation-pulse configuration, and uplink decimation and PRACH routing.
- Authored the firmware implementation guides for the NR symbol phase-compensation term of TS 38.211 section 5.4 (quadrant-folded trigonometric LUT, 4097-entry table, 21-bit minimum phase accumulator, numerology-dependent parameters, since a wrong term shows up as a rotated constellation; revised through v1.3) and for RFSoC ZU67DR pre-emphasis (per-subcarrier 16-bit LUTs flattening pulse-shaping passband droop for 5 to 30 MHz, with the LTE and LTE plus NB-IoT edge cases per TS 38.104 section 5.7.3).

- Wrote the uplink DFE receiver test plan for LTE, NR and MSR against TS 36.141 and TS 38.141: reference sensitivity, dynamic range, in-channel and adjacent-channel selectivity, and narrowband, in-band and out-of-band blocking, with bottom, mid and top frequency coverage per band and VRB-offset sweeps.
- Designed 8-block PRACH detection within the Xilinx PRACH core's 4K-FFT limit by cascading two 4K FFTs as a filter bank with per-block phase-rotation correction, and mapped LTE and NR PRACH subcarriers onto the core's FFT sizes and decimation ratios.
- Ran filter design, CFR simulation and cancellation-pulse generation for uplink, downlink and PRACH DFE firmware: a hard-clipper threshold sweep in 0.1 dB steps that set the 7.8 dB PAR operating point for E-TM 3.1, a first- and second-difference slew-rate detector for post-IFFT overflow, and cancellation-pulse analysis delivered to a major OpenRAN program partner in 2022.
- Generated RTL stimulus vectors, integrated Xilinx hard-IP C-models, developed executable models for UVM testbenches, and wrote PCAP tooling to extract O-RAN C-plane and U-plane data for bit-accurate system modeling.

FLORIDA INTERNATIONAL UNIVERSITY Miami, Florida
Graduate Research Assistant *2018 to 2020*

- Developed digital and mixed-domain hardware-reduction algorithms for massive MIMO receivers, the basis of the dissertation and most of the 10+ IEEE publications, all on reduced-ADC array architectures.
- Implemented a 28 GHz digital beamforming array receiver with 800 MHz per channel on Xilinx RFSoC (ZCU111, ZCU1275, ZCU1285), cutting ADC count by 75% with frequency multiplexing, and showed a further 50% ADC reduction for 2D phased arrays over the air.

MATHWORKS Natick, Massachusetts
Engineering Intern *2019*

- Enhanced HDL Verifier workflows and developed Ethernet PHY-interface IP across Artix, Kintex and Virtex FPGAs; two awards in the fall 2019 intern hackathon.

THE UNIVERSITY OF AKRON Akron, Ohio
Graduate Research Assistant *2016 to 2018*

- DARPA, NSF, and AFRL-funded research on multidimensional RF systems: approximate-DFT beamforming cores and multidimensional delta-sigma ADC architectures for phased-array receivers.

SYNOPSYS INC. Colombo, Sri Lanka
Product Verification Intern *2015*

- Automated product-verification test cases in Perl across VHDL and SystemVerilog ASIC flows with Spyglass and Xilinx FPGAs.

INDEPENDENT AI SYSTEMS

- **Salient:** USMLE exam practice with an AI patient that never gives away the diagnosis. All case details are pre-written and checked, so the model cannot invent a result, and a leak guard blocks any answer that might reveal the diagnosis. Six model roles, each sized to its task; a per-call cost ledger with daily budgets; grading aligned with published exam rubrics. 700 unit tests and 24 browser journeys.
- **TaxLens:** Rebuilds a year's small-business books from raw bank and card statements into a locked ledger, financials, and tax worksheets (Schedule C, 1120-S, 1065, 1120). Routes each step to a model sized to its risk in a multi-agent pipeline. Each deduction carries an IRS citation, an evidence rating, and a confidence score. A Section 274(d) guard runs in code on every write; classifications are append-only and hashed on lock. In one real client year, it caught $10K of double-counted bounced payments that manual review had missed. 400+ unit tests. It does not file.

EDUCATION

FLORIDA INTERNATIONAL UNIVERSITY Ph.D., Electrical and Computer Engineering, 2020 — Miami, Florida
UNIVERSITY OF RUHUNA B.Sc. (Hons), Electrical and Information Engineering, 2016 — Galle, Sri Lanka
NATIONAL INSTITUTE OF BUSINESS MANAGEMENT A.S., Business Management, 2015 — Galle, Sri Lanka
Affiliations: IEEE, member since 2013; Tau Beta Pi Engineering Honor Society, 2019 to present

SELECTED PUBLICATIONS

- Frequency-Multiplexed Array Digitization for MIMO Receivers: 4-Antennas/ADC at 28 GHz on Xilinx ZCU-1285 RF SoC, IEEE Access, vol. 9, 2021.
- Spacetime Frequency-Multiplexed Digital-RF Array Receivers with Reduced ADC Count, IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 68, 2021.
- Massive-MIMO and Digital mm-Wave Arrays on RF-SoCs using FDM for M-Fold Increase in Antennas per ADC/DAC, 2021 IEEE Space Hardware and Radio Conference (SHaRC), 2021.
- Fast Radix-32 Approximate DFTs for 1024-Beam Digital RF Beamforming, IEEE Access, vol. 8, 2020.
- A Direct-Conversion Digital Beamforming Array Receiver with 800 MHz Channel Bandwidth at 28 GHz using Xilinx RF SoC, IEEE COMCAS, Israel, 2019.
- Multiport ADCs for Microwave Focal Plane Array Dish Receivers, IEEE International Symposium on Circuits and Systems, Italy, 2018.

10+ IEEE publications, an AFRL technical report, and a dissertation; full list at najathakram.info.