NAJATH AKRAM, PH.D.

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SUMMARY

Signal processing engineer specializing in 5G NR and LTE radio units, from algorithm design through silicon-facing verification. Owns the golden-model estate for multiband O-RAN RRUs at Airspan: DFE, CFR, PRACH, and fronthaul-accurate uplink and downlink chains validated bit-exactly against AMD/Xilinx IP. Builds AI-assisted engineering pipelines that compress verification and porting cycles from weeks to days. Ph.D. in reduced-hardware beamforming receivers with nine IEEE publications.

CORE SKILLS

Wireless Systems: 5G NR / LTE PHY, O-RAN fronthaul (Split 7-2x, WG4 CUS-plane), 3GPP 38-series, multiband TDD / FDD RRU architecture, massive MIMO, EVM / ACLR / PIM analysis

DSP and Modeling: DFE design (DUC / DDC, NCO, channel filters), CFR and cancellation-pulse design, PRACH detection, MRC / IRC combining, polyphase filter banks, fixed-point and bit-exact modeling, BFP compression

Platforms and Tools: MATLAB / Simulink (5G, LTE, HDL toolboxes), AMD/Xilinx RFSoC and DFE IP C-models, Python, MATLAB Compiler, PCAP and fronthaul analysis, Git

AI Engineering: Anthropic Claude API and Agent SDK, multi-agent development pipelines, AI-assisted verification and cross-language porting with ground-truth regression

EXPERIENCE

AIRSPAN NETWORKS Houston, Texas

Signal Processing Engineer *2025-Present*

- Lead system and verification modeling for multiband LTE / 5G NR (TDD / FDD) O-RAN RRUs: own the versioned golden-model executables (downlink, uplink, low-PHY, PRACH) that generate bit-exact RTL and fronthaul test vectors against AMD/Xilinx DFE IP C-models for firmware sign-off.
- Built the PRACH receive-chain model covering LTE FDD and full NR FR1 (long and short preambles, all 256 3GPP configuration indices, FDD and TDD), backed by a 386-check automated verification harness; root-caused occasion-timing and cyclic-prefix defects to the sample.
- Developed an O-RAN fronthaul PCAP power analyzer implementing O-RAN WG4 CUS measurement definitions with automatic eAxC, SCS, and compression detection; verified to 0.000 dB against an independent oracle, calibrated within 0.06 dB of reference captures, and packaged as a standalone Windows executable for lab teams.
- Rebuilt that analyzer in pure Python through an AI-agent plan, implement, and review pipeline (five spec-driven cycles), cutting per-capture analysis from roughly 45 seconds to 3 seconds with regression tests pinning every result within 0.05 dB of MATLAB ground truth.
- Ran 29 production debug engagements over 18 months across TDD / FDD bring-up, PRACH, observation-receiver, and gain issues, working lab and field captures from Ericsson, VIAVI, and partner test stacks down to root cause.
- Designed a bit-accurate firmware model of intelligent uplink MRC combining for O-RAN shared-cell DAS (up to 4 RUs x 8 antennas) with fixed-point channel estimation and CORDIC delay and phase tracking; matched the floating-point reference within 0.01 dB SINR and held 34 dB SINR where equal-gain combining collapsed below 8 dB.
- Wrote a from-scratch NR uplink per-UE demodulator driven entirely by decoded O-RAN fronthaul captures (bit-exact Gold-sequence DMRS regeneration from C-plane configuration, per-RE MMSE equalization), paired with a Monte-Carlo simulator comparing seven uplink combining schemes under 3GPP TR 38.901 channels with TS 38.213 power control.
- Modeled an 18-channel polyphase filter bank for an O-RU spectrum-sensing board (691.2 Msps input, 18 x 38.4 Msps channels) feeding an ML signal classifier on NVIDIA Orin; two independently built implementations proven bit-identical.
- Built a PIM range analyzer flagging third and fifth-order intermodulation hits across single, dual, and tri-band configurations, and contributed system modeling and standards-grounded gap analysis to Airspan 6G research.

JABIL INC. Warren, New Jersey | Houston, Texas

Principal Design Engineer (Wireless Systems) *2023-2024*

Lead Design Engineer (Wireless Systems) *2021-2023*

Senior FPGA Engineer (Wireless Systems) *2020-2021*

- Led software and firmware workstreams for LTE and 5G NR O-RAN RRUs, defining NR implementation requirements and producing the architecture and implementation documents the digital design team built to.
- Performed filter design, CFR simulation, cancellation-pulse generation, and end-to-end system modeling for uplink, downlink, and PRACH DFE firmware across single, dual, and tri-band LTE / 5G NR radios.

- Delivered CFR cancellation-pulse analysis for a major OpenRAN program partner (2022) and contributed to strategic decisions on massive MIMO implementation and O-RAN functional splits.
- Generated stimulus vectors for RTL simulation, integrated Xilinx C-models for hard IP, developed executable models for UVM testbenches, and wrote PCAP tooling to extract O-RAN control and user-plane data for bit-accurate system modeling.

FLORIDA INTERNATIONAL UNIVERSITY Miami, Florida
Graduate Research Assistant *2018-2020*

- Developed digital and mixed-domain hardware-reduction algorithms for massive MIMO receivers, the basis of nine IEEE publications and a dissertation on reduced-ADC array architectures.
- Implemented a digital beamforming array receiver with 800 MHz per channel at 28 GHz on Xilinx RFSoC platforms (ZCU111, ZCU1275, ZCU1285), cutting ADC count by 75% with a frequency-multiplexed approach, and demonstrated a further 50% ADC reduction for 2D phased arrays with over-the-air validation.

MATHWORKS Natick, Massachusetts
Engineering Intern *2019*

- Won two awards in the fall 2019 intern hackathon; enhanced HDL Verifier and developed Ethernet PHY-interface IP designs across Artix, Kintex, and Virtex FPGAs.

THE UNIVERSITY OF AKRON Akron, Ohio
Graduate Research Assistant *2016-2018*

- Conducted DARPA, NSF, and AFRL-funded research on multidimensional RF systems: approximate-DFT beamforming cores and multidimensional Delta-Sigma ADC architectures for phased-array receivers.

SYNOPSYS INC. Colombo, Sri Lanka
Product Verification Intern *2015*

- Automated product-verification test cases in Perl across VHDL and SystemVerilog ASIC flows with Spyglass and Xilinx FPGAs.

INDEPENDENT AI SYSTEMS

- TaxLense: AI tax engine that reconstructs ledgers from raw bank statements and classifies deductions with IRC citations through a multi-agent Anthropic API pipeline; evidence-tiered claims, an append-only audit ledger, per-call cost tracking, and 400+ unit tests.
- Salient: conversational clinical-case simulator for OSCE exam preparation with AI patient role-play over deterministic case data, per-user daily cost budgets, and durable call logging.
- RouteFlow: multi-tenant delivery SaaS (NestJS, Next.js, React Native) with 13 feature modules, live order tracking, and CI/CD to production infrastructure.

EDUCATION

FLORIDA INTERNATIONAL UNIVERSITY Miami, Florida
Ph.D., Electrical and Computer Engineering, 2020

UNIVERSITY OF RUHUNA Galle, Sri Lanka
B.S. (Hons.), Electrical and Information Engineering, 2016

NATIONAL INSTITUTE OF BUSINESS MANAGEMENT Galle, Sri Lanka
A.S., Business Management, 2015

Affiliations: IEEE, Member since 2013 | Tau Beta Pi Engineering Honor Society, 2019 to present

SELECTED PUBLICATIONS

- Digital and Mixed Domain Hardware Reduction Algorithms and Implementations for Massive MIMO, Ph.D. dissertation, Florida International University, 2021.
- Frequency-Multiplexed Array Digitization for MIMO Receivers: 4-Antennas/ADC at 28 GHz on Xilinx ZCU-1285 RF SoC, IEEE Access, vol. 9, 2021.
- Spacetime Frequency-Multiplexed Digital-RF Array Receivers with Reduced ADC Count, IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 68, 2021.
- Fast Radix-32 Approximate DFTs for 1024-Beam Digital RF Beamforming, IEEE Access, vol. 8, 2020.
- Multi-Beam RF Aperture Arrays Using Multiplier-less Approximate FFT, AFRL Sensors Directorate technical report AFRL-RY-WP-TR-2017-0144, 2017.

Nine peer-reviewed publications in total; full list at najathakram.info.